

REMARKS

Claims 1-8 are pending.

A new drawing is submitted for Fig. 1 that amends the term "use frequency counter" to "use frequency count". This should satisfy the objection to the drawings.

Claim 8 is proposed to be amended to overcome the §112 rejection.

Claim 1-4 stand rejected over Fig. 4 of the present Specification. In the June 29, 2004 response to the Office Action, applicants had argued that the conventional semiconductor test apparatus did not comprise a pattern file use frequency table memory. The Examiner asserts that the prior art structure is capable of performing the intended use of such a table.

As described beginning at page 1, line 23 of the Specification, in the conventional semiconductor test apparatus shown in Fig. 4, the control unit 40 stores the pattern files in the DISK 42, contained in the test apparatus 41. For testing, the pattern files are transferred to the executive memory, and the tests are performed by picking up a test pattern in the executive memory, when the test pattern is present in the executive memory. When a new test pattern which is not included in the test pattern set is to be used, the new test pattern is transferred to the executive memory. However, when the capacity of the executive memory is insufficient for accepting the new test pattern, the control unit in the conventional apparatus technique first erases all of the stored original data. Then a new pattern data set including the new pattern data must be transferred to the executive memory for executing tests of semiconductor devices with the new test pattern. The original data set is lost.

The present semiconductor test apparatus and method overcomes this deficiency. It generates and uses a use frequency table memory for storing a table showing the relationship between each of pattern files and the number of times (frequency) the data of each of the files is used. When a new test pattern is to be used and the capacity of the executive memory is insufficient for storing and executing such new test pattern, the control device deletes a pattern file having the lowest use frequency by referring to the use frequency table memory. The new test pattern can be transferred to the executive memory

for use without erasing all pattern data in the executive memory and the semiconductor test can be carried out efficiently. That is, only one data pattern is erased instead of erasing the complete original set of data patterns as in the method/apparatus of Fig. 4.

Claim 1 is proposed to be amended by the addition of elements of the present semiconductor test apparatus, which differentiate the present invention from the prior art of Fig. 4. These elements include a control unit for controlling the semiconductor test apparatus, a disc apparatus and a buffer memory that store a plurality of pattern files transferred from an external memory, and an executive memory comprising a pattern memory, an MIC memory, and an SPG memory for storing test patterns and executive tests for each type of semiconductor. There also is recited a counting device that counts the number of times pattern data is used for each of said pattern files and a control unit that produces the pattern file use frequency table discussed above. The latter feature clearly is not shown in Fig. 4. Claims 2-4 depend from claim 1 and recite further features of the test device.

Accordingly, claims 1-4 as now amended patentably distinguish over Fig. 4 showing the conventional technique.

Claims 5-8 stand rejected over Enoki, et al., U.S. 5,873,085 and Tonaga, et al., U.S. 5,479,657. Claim 5 is an independent method claim from which claims 6-8 depend. The Examiner asserts that the Enoki reference is reasonably pertinent in that it improves the data storage capabilities in the same manner claimed by applicants.

The Enoki reference discloses a virtual file management system, constructed with a plurality of servers and a plurality of terminals that share file services provided by the servers. However, the Enoki reference does not teach the semiconductor test apparatus of the present invention comprising a disc apparatus, a buffer memory and an executive memory comprising a pattern memory, an MIC memory, and an SPG memory. Enoki also does not teach or suggest the claimed step of preparing a pattern file use frequency table memory and storing this table which shows the relationship between a pattern data and the number of times the pattern data is used. As explained above, this permits efficiently carrying out semiconductor tests using a new test pattern by introducing the new test

pattern only by replacing a test pattern having the lowest use frequency, when the capacity of the executing memory is insufficient.

Therefore, the invention as set forth in claims 5-8 is not at all similar to what is disclosed in the Enoki reference.

Tonaga discloses a method and system for sorting count information in a computer. Frequency of usage of count information is first determined and the frequency of usage is added to count information. The count information with the frequency information is then arranged in ascending or descending order in a memory in order to sort count information in an ascending or descending order.

Tonaga does not teach a semiconductor test apparatus in which the number of times pattern data is used and counted and a pattern file use frequency table is prepared showing the relationship between each of pattern files and the number of times the pattern file is used. It also does not show the subject matter of claims 7 of erasing the pattern file having the lowest frequency when the capacity of the executive memory is insufficient for storing a new pattern file for executing the semiconductor test. Tonaga only teaches the use frequency information of count information and does not teach to erase the pattern file having the lowest frequency. Therefore, the combination of Tonaga with Enoki does not render claims 5-8 obvious.

There appears to be no basis to make the combination of these two references. That is, Tonaga has no relationship to a semiconductor test apparatus, and there is no teaching in Enoki that a frequency use table is either needed or even desired. Therefore, claims 5-8 are patentable and should be allowed.

A new apparatus claim 9 and method claim 10 are submitted. Claim 9 draws on features of claims 1-4 and combines them. Similarly, method claim 10 draws on features of claims 5-8 and combines them. Therefore, no new matter is added and no new issues are raised.

The amendment should be entered since it clearly places the application in condition for allowance. It does not raise any new issues.

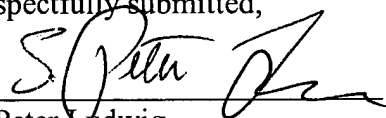
If the amendment is not entered as placing the application in condition for allowance, then its entry is requested for purposes of appeal.

Prompt and favorable action is requested.

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Respectfully submitted,

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AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to .

Attachment: Replacement sheet